Low-Temperature Fabrication of Si Thin-Film Transistor Microstructures by Soft Lithographic Patterning on Curved and Planar Substrates

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We demonstrate the use of micrometer-scale polymer molding, a soft-lithographic patterning technique, as a means to fabricate amorphous silicon thin-film transistors (TFTs). Two different TFT architectures were fabricated and tested—a common gate, common channel architecture for single-level patterning on a spherically curved glass substrate—and an isolated channel, inverted, staggered architecture with multilevel pattern registration on a planar glass substrate. The silicon and silicon nitride films are deposited by reactive magnetron sputtering, allowing all film depositions to be carried out at temperatures at or below 125 °C, and making this fabrication process a candidate for use on plastic or other thermally sensitive substrates. We discuss the performance of polymer molding as a patterning technique for thin-film microstructures on both planar substrates and on substrates with three-dimensional curvature.

Introduction

Polymer molding that uses capillary action to fill a patterned elastomeric mold, commonly referred to as "micromolding in capillaries" or MIMIC, is an attractive alternative or complementary technique to thin-film patterning by conventional photolithography,[1−3] and has been used to fabricate a variety of microelectronic devices.[4−8] In seeking to explore and extend the range of processing conditions for which polymer molding might serve as an effective patterning technique, we undertook the fabrication of model arrays of hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs). To test the limits and general utility of this thin-film patterning method, these arrays were fabricated on both planar and spherically curved substrates using two different TFT architectures.

TFTs were chosen as test structures for several reasons. First, TFTs are extremely useful devices in diverse areas of technology and can be made with a variety of architectures, including ones that can conveniently be fabricated on curved substrates.[9] For example, TFTs are used to address the pixels in flat panel displays and have potential uses in other device applications.[10−13] Second, TFTs are composed of thin films that can be deposited readily at low temperatures (here as low as 125 °C), and thus can be fabricated on plastic or other unconventional substrates.[8,14−18] Third, fabricating TFT structures allows us to test the performance of polymer molding as a micrometer-scale patterning technique for devices on nonplanar (here, spherically curved) substrates.

Our group has demonstrated excellent a-Si:H TFTs using low-temperature reactive magnetron sputtering (RMS),[14,19−20] a technique in widespread industrial use for thin-film deposition. The device designs of interest in this study require the patterning of metal and silicon nitride by wet-etching and lift-off methods. The lift-off of micromolded polymer templates, which has been

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extensively studied in the patterning of metal microstructures,[2,4−6,21] has not been examined as a means to prepare devices in reactive sputter-deposition conditions, including high-vacuum, mildly elevated temperature, and a plasma environment.

Polymer molding is a powerful tool for fabricating device arrays on nonplanar substrates, as the flexible elastomeric molds can be brought into conformal contact even with substrates of steep curvature.[2,21] Soft-lithography has been applied to a variety of nonplanar substrates in the past,[3,22−23] but fabricating multilayered electronic devices on spherically curved substrates has yet to be demonstrated, primarily due to the difficulty of achieving multilevel feature registration on a surface with three-dimensional curvature.

There are, however, numerous scientific and technological incentives for patterning spherically curved substrates.[24,25] For example, the human eye focuses images on a nearly spherically curved retina which neatly accommodates the relatively simple optics of the eye's lens. Similarly, a Schmidt telescope uses a curved detector (film plate) to minimize the need for complex correction optics that would be required to focus images on a planar detector surface.[26] Curved detector arrays based on solid-state devices, however, are not generally available. These examples suggest a need to develop methods for fabricating multilevel thin-film devices in nonplanar geometries.

In this study, to obviate the need for multilevel registration on a curved-surface array, we adopted a TFT architecture that required only one mask level. This TFT architecture, referred to as the "common gate/channel" structure (Figure 1), uses a single Al layer as a monolithic gate electrode for all of the source/drain contacts in the array rather than using individually addressable gate lines. Likewise, the semiconductor (channel) layer is also common to all source/drain contacts on the substrate. While this architecture does not yield optimal electrical results due to current spreading in the common gate and channel regions,[27] it was chosen for its suitability as a test structure for patterned thin-film devices on spherically curved substrates. In this work, we sought to fabricate TFT devices with feature sizes on the order of those used in commercial display technology, yet within the resolution limits of rapid prototyping fabrication methods that use laser-printed transparency sheets as mask patterns for fabricating the MIMIC mold masters (typically ∼20 μm). We should note, however, that MIMIC can be used to fabricate features as small as 1 μm.[3]

To further test these processing methods, we also fabricated TFTs with an inverted, staggered architecture supported on a planar glass substrate. These structures, like commercial TFTs, have channel regions

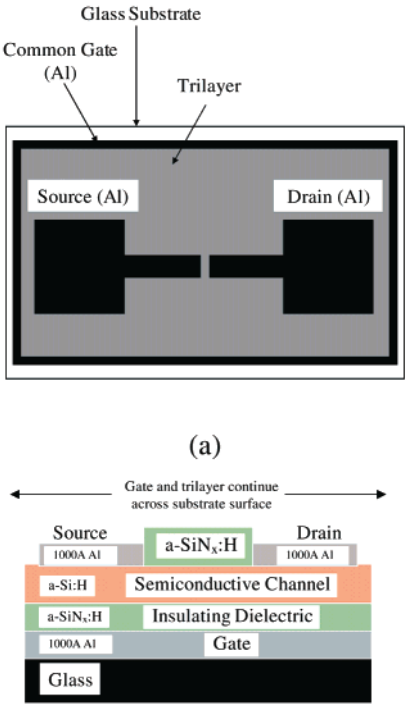

Figure 1. (a) Top view of the common gate/channel TFT architecture. (b) Cross-sectional view of the common gate/channel TFT architecture.

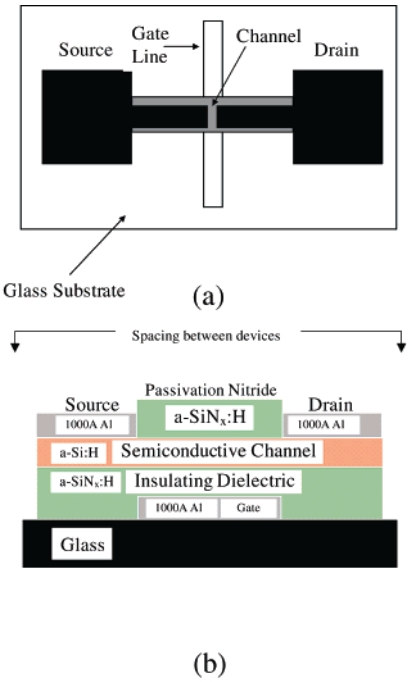

Figure 2. (a) Top view of the isolated channel, inverted, staggered TFT architecture. (b) Cross-sectional view of the isolated channel, inverted, staggered TFT architecture.

that are isolated to a single device. The gate electrodes were patterned as a series of Al lines. The isolated channel device architecture is shown schematically in Figure 2 and requires three levels of pattern registration. Taken together, the studies of common gate/channel TFTs and isolated channel TFTs have helped to identify key processing issues that must be addressed

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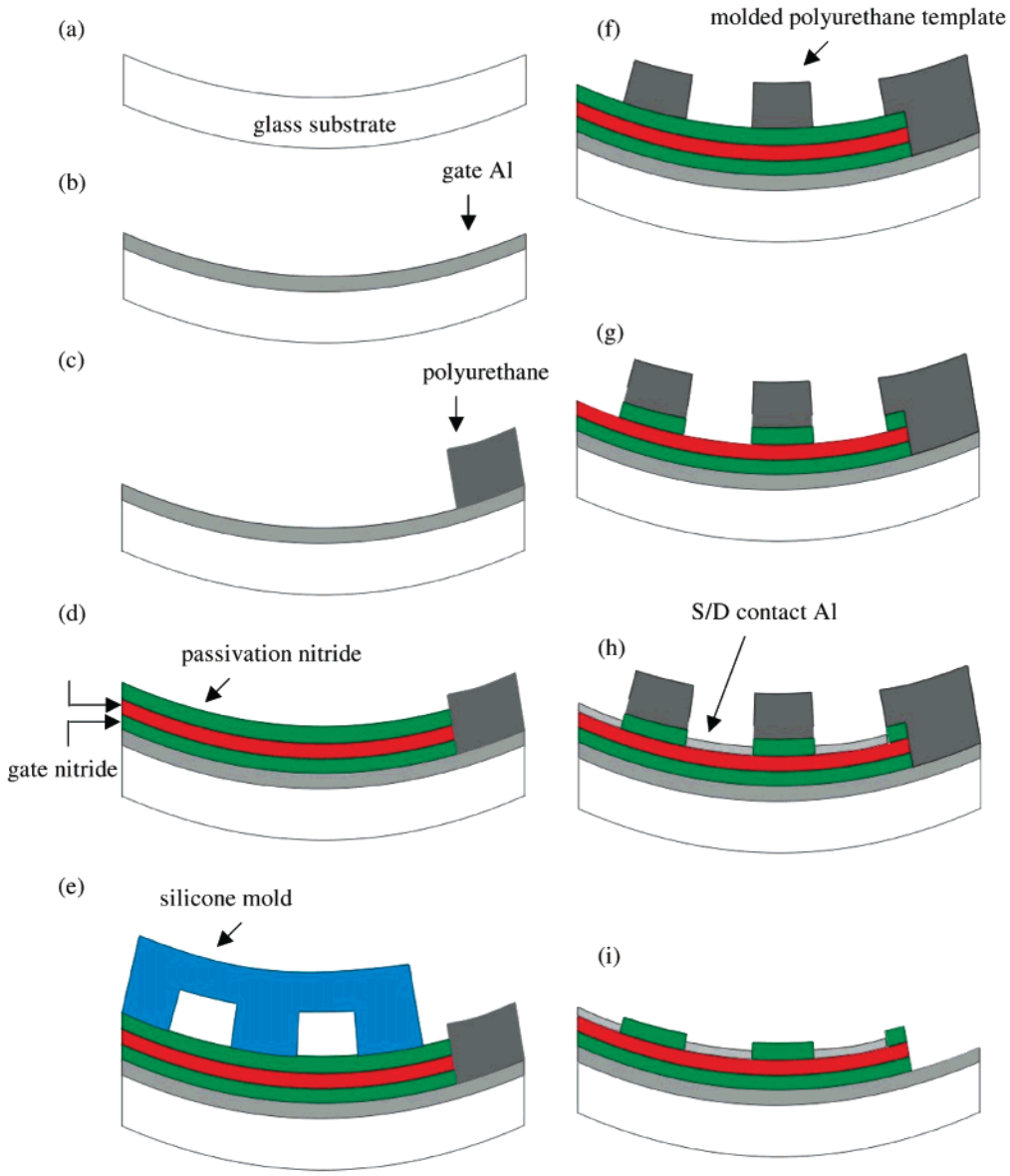

Figure 3. Cross-sectional schematic of the fabrication steps for microstructures with the common gate/channel TFT architecture on a spherically curved substrate (diagrams are not drawn to scale): (a) spherically curved glass substrate; (b) deposition of the common Al gate by thermal evaporation; (c) physical masking of the gate contact region; (d) three-step RMS deposition of gate dielectric (~3000 Å of a-Si_3N_4:H), semiconductor layer (~1000 Å of a-Si:H), and passivation layer (~3000 Å of a-Si_3N_4:H); (e) silicone mold contacts the substrate; (f) polyurethane precursor fills the channels of the silicone mold, is cured, and the mold is removed; (g) passivation nitride is etched to create source/drain contact windows to the a-Si:H layer; (h) source/drain contact metallization is done by thermal evaporation of Al (although not shown in the diagram, Al also coats the polyurethane template on the substrate); (i) polyurethane template lifted off in a CH_2Cl_2/CH_3OH solution. The gate contact pad is on the far right side of the substrate.

in order to realize multilevel pattern registration on spherically curved substrates.

Experimental Section

The method used to fabricate common gate/channel TFT microstructures on a spherically curved glass substrate is schematically illustrated in Figure 3. A 1000 Å thick film of Al was evaporated onto the concave side of a 1 × 1 $in.^2$ glass substrate cut from a watchglass. This substrate possessed a radius of curvature of ~10 cm. The surface of the glass substrate was cleaned prior to use with acetone, 2-propanol, water, and more 2-propanol, followed by drying with nitrogen and 10 min of low-intensity (~1 mW/cm^{-2}) UV exposure in air (mercury vapor lamp, BHK Inc.). Following the metal evaporation, the substrate was annealed for 15 min at 475 °C to promote adhesion and to prevent subsequent peeling of the Al film from the substrate. Although not examined explicitly in this study, other low-temperature methods can likely be used, if necessary, to promote adhesion of the gate electrode layer to temperature-sensitive substrates. When the substrate had cooled, a 0.5 cm wide stripe of a UV-curable polyurethane prepolymer (NEA 121, Norland Products) was applied along one edge of the substrate surface to physically mask the underlying Al from further deposition. This masking is necessary when fabricating the common gate structure in order to establish an electrical contact to the Al gate.

After the polyurethane was cured for 3 min under a low-intensity UV source, the substrate was introduced to a three-chamber RMS deposition system,[14] where we deposited a 3000 Å thick film of hydrogenated amorphous silicon nitride (a-SiN_x:H) for the gate dielectric, a 1000 Å thick film of a-Si:H for the active layer, and a 3000 Å thick film of heavily hydrogenated a-SiN_x:H for the passivation layer at a substrate temperature

Table 1.

	temp. (°C)	time (min)	*P* [Ar] (mTorr)	*P* [H_2] (mTorr)	*P*[N_2] (mTorr)	total pressure (mTorr)
gate nitride	125	60	1.0	0.4	1.5	2.9
a-Si:H	125	6	1.5	0.6	0	2.1
passivation nitride	125	60	1.5	0.4	2.6	4.5

of 125 °C. The nitride films were grown in one chamber using an ($Ar/H_2/N_2$) plasma generated by an ENI RPG-50A power supply in pulsed DC mode, where the pulse frequency = 100 kHz, reverse bias supply voltage = +75 V, and duty cycle = 30%. A pulsed deposition protocol was used to prevent silicon nitride buildup on the target. Silicon films were grown in an isolated adjacent chamber using an (Ar/H_2) plasma in static DC mode. Finally, the passivation nitride layer was deposited in the first chamber using an excess of N_2 to promote growth of a sparse, columnar microstructure that could easily be etched. A summary of the growth conditions is given in Table 1 below. The composition, microstructure, and electronic properties for films obtained using these deposition conditions have been described in detail elsewhere.[14,19−20,28]

Following film deposition, a resist template for the definition of the source/drain contacts was created by MIMIC. A "rapid prototyping" method was used to fabricate the patterned silicone molds used in the MIMIC process, as has been described in detail elsewhere.[1−3] A patterned silicone mold (poly(dimethylsiloxane), Dow Corning, Sylgard 184) was brought into contact with the concave face of the substrate. The polyurethane precursor was then applied along an open edge of the mold, drawn into the recessed channel regions of the mold by capillary action, and cured for 12 min under a mercury vapor UV source. Following curing, the mold was peeled from the substrate, leaving a polyurethane pattern on the substrate surface, roughly 30 μm high. Within the template pattern, the distance between source and drain contacts was intentionally varied between 60 and 120 μm in regular increments. The contacts themselves were approximately 200 μm × 200 μm to facilitate probe placement for electrical measurements.

Following the molding of the polymer template, the sample was submerged in a 6:1 NH_4F/HF buffered etching solution for 2 min, rinsed with water and 2-propanol, and dried under nitrogen flow. After etching, the sample was immediately transferred to an evaporation bell jar, where 1000 Å of Al was deposited to form contacts to the Si channel layer. Following Al deposition, the substrate was immersed in a 5:1 CH_2Cl_2/CH_3OH solution for 10 min to remove the polyurethane from the substrate surface. This completed the fabrication of the common gate device array.

The method used to fabricate isolated channel thin-film transistors on a planar glass substrate is illustrated schematically in Figure 4. A patterned silicone mold was brought into contact with the surface of a 1 × 1 in.^{2}, planar glass substrate, cleaned prior to use as described above. A patterned polyurethane template for the deposition of the Al gate lines was then formed by the MIMIC technique. A 1000 Å thick film of Al was then evaporated onto the sample, followed by polymer liftoff in CH_2Cl_2/CH_3OH. The width of the gate lines was intentionally varied from 60 to 120 μm in regular increments across the array.

Following the formation of the Al gate line, alignment of the mold defining the isolated trilayer region of the TFT structures was carried out using a Karl Suss contact aligner.[4,29] The trilayer template pattern was brought into contact with the substrate while maintaining registration with Al gate lines on the substrate. A second MIMIC step was then performed, after which the sample was placed in the series of interlocked RMS chambers for trilayer deposition. Following deposition of the trilayer, as described above, the polymer template was removed by liftoff in CH_2Cl_2/CH_3OH.

A third and final patterning step was then performed to define the source/drain contacts. Mold alignment on the substrate was, as above, followed by the polymer molding procedure, which, in turn, was followed by consecutive etching, Al evaporation, and polymer liftoff steps, as described above for the common gate/channel device structures. As with the common gate/channel devices, the distance between source and drain contacts was intentionally varied between 60 and 120 μm in regular increments within the template pattern, and the contacts themselves were approximately 200 μm × 200 μm to facilitate probe placement for electrical measurements. This completed the fabrication of the isolated TFT arrays.

Scanning electron micrographs of sample fracture cross sections were obtained on a Hitachi S-4700 field emission gun scanning electron microscope. Electrical measurements were performed using a probe station connected to a HP4145B semiconductor parameter analyzer, with commercial data collection and analysis software (Hewlett-Packard, IC−CAP).

Results and Discussion

The requirements for etching silicon nitride in the fabrication of the TFT devices were a significant factor influencing our choice to use MIMIC as a patterning tool in this study. The inks available for patterning etch resists by contact printing do not generally perform well in HF-based etching solutions or under reactive ion etching (RIE) conditions.[3,30−31] From our use of MIMIC as a patterning tool, we identified and solved several potential obstacles to patterning thin-film microstructures via polymer molding. The first issue is that the silicone molds used to define the MIMIC template pattern do not always cure completely, and as a result, may leave an oligomeric residue on the surfaces they contact. Such contamination greatly reduces the adhesion of subsequently deposited material, which can be a significant problem. We, however, found it convenient and effective to place the molds face-up directly under a UV light source for 5−10 min following curing to ensure the removal or conversion of any residual oligomer on the mold surface. The mold was then used without problem to pattern the polyurethane template on the substrate

More generally, though, we found that the adhesion of Al base layers to the glass substrates used in this work was subject to unpredictable failures during subsequent stages of the fabrication. Rather than examining specific chemistries to promote this adhesion, we chose instead to simply anneal the sample following the Al evaporation step. The rest of the fabrication was then carried out normally, and the Al remained strongly adhered to the substrate during subsequent template liftoff steps.

Another potential problem with using MIMIC as a patterning tool for a-Si:H and a-SiN_x:H films was the possibility that the UV radiation used to cure the polyurethane would generate dangling bond defects in

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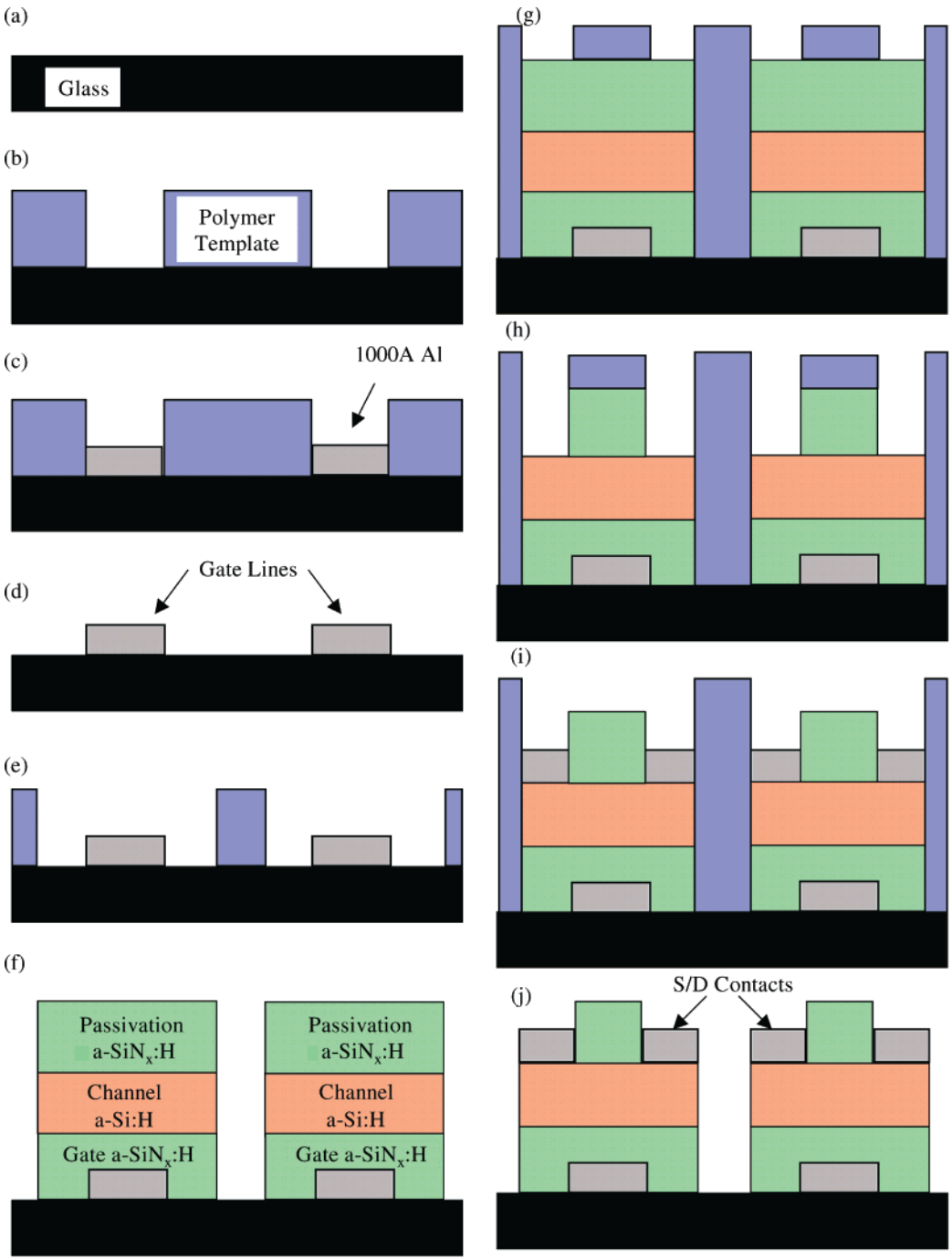

Figure 4. Cross-sectional schematic of the fabrication steps for microstructures with the isolated channel, inverted, staggered TFT architecture on a planar substrate (diagrams are not drawn to scale): (a) planar glass substrate; (b) definition of the gate line pattern via molding of a photocured polyurethane template; (c) gate lines deposited by thermal evaporation of Al (although not shown in the diagram, Al also coats the polyurethane template on the substrate, as is also the case in part i); (d) polyurethane removed in CH_2Cl_2/CH_3OH solution; (e) alignment and polymer molding to define an isolated channel deposition pattern; (f) three-step RMS deposition of gate dielectric (~3000 Å of a-Si_3N_4:H), semiconductor layer (~1000 Å of a-Si:H), and passivation layer (~3000 Å of a-Si_3N_4:H) trilayer, followed by removal of the polyurethane deposition template (not shown); (g) alignment and polymer molding to define the etching and metallization pattern for source/drain contact formation; (h) passivation a-SiN_x:H layer etched to open contact windows to the a-Si:H channel layer; (i) source/drain contact metallization is done by thermal evaporation of Al; (j) liftoff of the polyurethane leaving isolated channel microstructures with the inverted, staggered TFT architecture.

the a-Si:H and a-SiN_x:H films and thereby degrade the electrical performance of the devices.[32] This obstacle was obviated by using a photocurable polyurethane prepolymer that did not require high-energy exposures to effect the cure. As a result, the exposure to UV radiation was kept within the range used for the photolithographic patterning of commercial-grade TFTs.

Arrays of TFTs were fabricated in two different architectures on spherically curved and planar glass substrates. The curved TFT arrays were fabricated in the common gate/channel architecture shown in Figure 1 (Figure 1b is shown as a planar, rather than curved,

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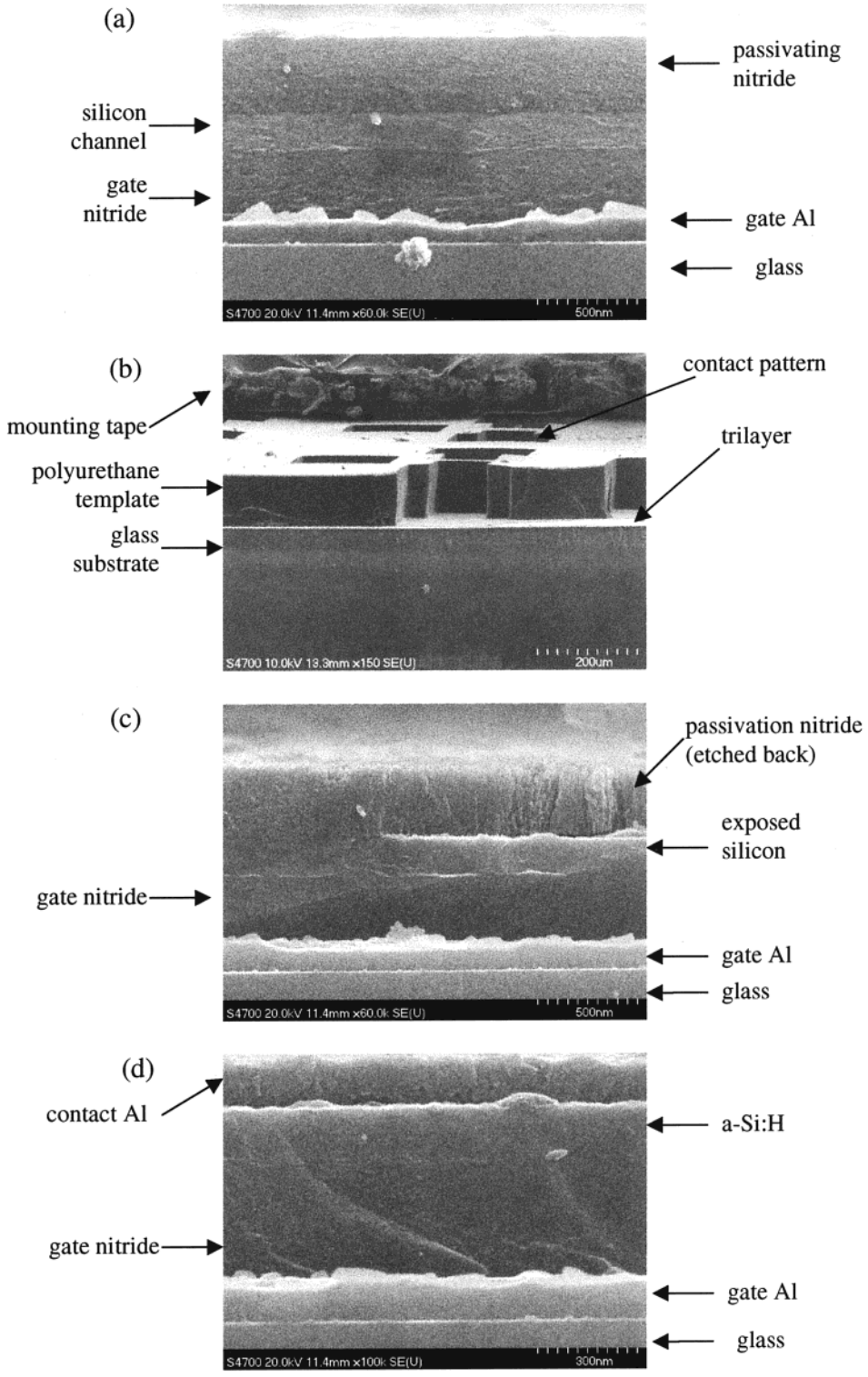

Figure 5. Fracture cross-section SEM micrographs showing common gate/channel microstructures following: (a) gate metallization and trilayer deposition (Figure 3d); (b) polymer molding to define source/drain contact pattern (Figure 3f); (c) etching of the passivation nitride (Figure 3g); (d) contact metallization (Figure 3i).

structure for the sake of readability). The critical advantage of this architecture over an isolated device architecture is that it requires only one mask level, allowing for TFT fabrication on a spherically curved substrate without the additional complication of pattern registration of multiple mask levels. Even without pattern registration, patterning by MIMIC on a curved substrates presents special challenges. For example, the mold must be flexible enough to conform to the curvature of the substrate surface, yet stiff enough to preserve the integrity of the pattern. Typically, we used elastomeric PDMS (poly(dimethylsiloxane), Dow Corning Sylgard 184) molds no more than a few millimeters thick. As the curvature of the substrate surface increases, so too does the difficulty of patterning it using MIMIC. Other soft-lithographic techniques, however, such as

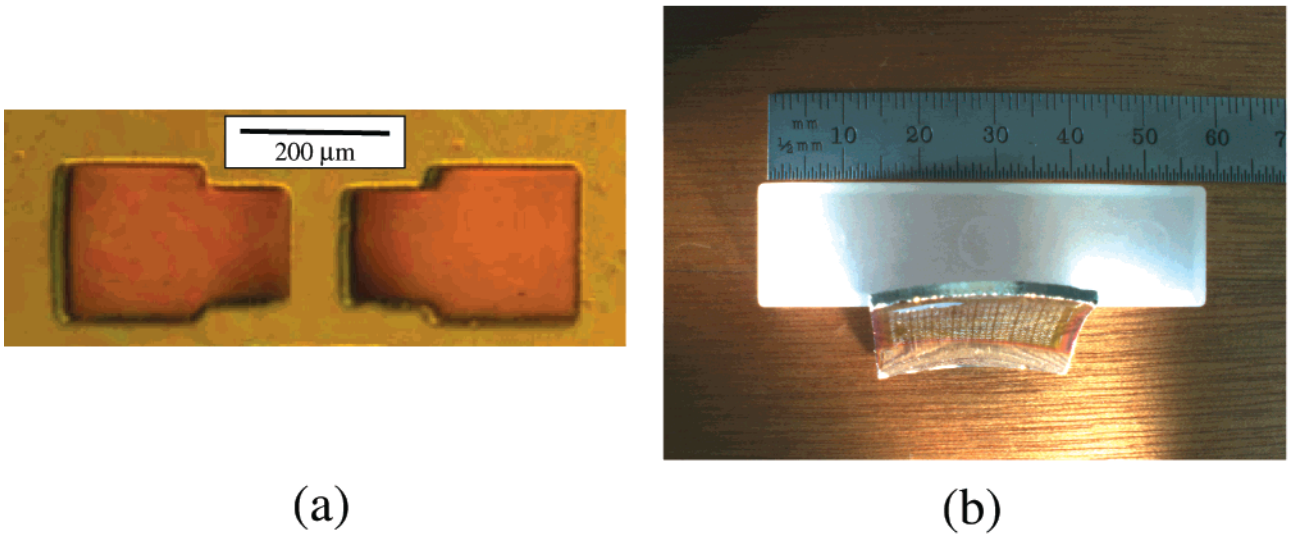

Figure 6. (a) Top view of a single completed common gate/channel TFT structure on a spherically curved glass substrate. (b) TFT array.

contact printing, which does not rely on capillary flow within a mold, can be adapted easily to accommodate highly curved surfaces.[3,23,33,34]

A schematic illustration of the fabrication method for the common gate/channel devices is shown in Figure 3. Figure 5 shows SEM images of common gate/channel device cross sections at progressive stages of fabrication. The polyurethane resists obtained by MIMIC produce high aspect ratios and excellent vertical wall profiles. Figure 6 shows optical micrographs of a completed common gate/channel TFT (Figure 6a) and of a completed device array on a spherically curved glass substrate (Figure 6b).

Figure 7 shows the electrical characteristics of the transistors. Nonideal electrical behavior is observed due to the simplified (common gate/channel) architecture in which these devices were fabricated. We have observed similar electrical behavior in planar TFTs fabricated with this architecture but using resists patterned by photolithography.[35] Ideal behavior is characterized by output curves similar in shape to those shown in Figures 7a and 8a (but intersecting at the origin), and by transfer curves similar in shape to those presented in Figures 7b and 8b (but with lower gate current relative to source current).[9] The most significant contributor to the deviation from ideal transistor behavior is the tendency of common gate/channel devices to exhibit current spreading, resulting in high leakage currents,[27,36] which are evident in the data presented in Figure 7. We also fabricated common gate/channel devices on a planar glass substrate to provide a system for comparison. Representative electrical properties of the planar device arrays are shown in Figure 8 and are similar to those that we and others have previously observed in common gate/channel devices.[35,36]

In common gate/channel device arrays, the gate and semiconductor layers are not confined to a limited area immediately below and between the source/drain contacts. For this reason, the current detected at the gate electrode is due not only to the relatively small current that penetrates the gate dielectric in the immediate vicinity of the device but also includes a much larger contribution from the current paths generated across the entire substrate as a direct result of the general wide-area biasing of the common gate beneath the monolithic semiconductive channel. This conclusion was confirmed by a direct measurement of the leakage current through the gate nitride alone, as shown in Figure 9a, which is several orders of magnitude lower than the gate current observed in the common gate/channel TFTs. Figure 9b shows the test structure used to measure the leakage current through the gate nitride alone. The leakage current shown in Figure 9a compares well to the previously reported values of $\sim 10^{-8}$ A/cm^2 at 3×10^6 V/cm for planar nitride layers deposited at 125 °C,[14] which is considered acceptable for production devices.

Current spreading across a device array like that seen in the common gate/channel TFTs can be minimized by electrically isolating each device in the array. Therefore, the second of the two device architectures that we fabricated was an inverted, staggered TFT with an isolated channel and a gate line common only to devices in one row of the array, as shown in Figure 2. Because multiple mask levels are needed for the fabrication of the isolated channel device architecture, these TFT arrays were fabricated on a planar glass substrate as an initial test to simplify pattern registration. The fabrication process is illustrated schematically in Figure 4. The isolated channel devices are shown at progressive stages of fabrication in Figure 10. The metal gate lines derived from MIMIC (Figure 10a) had excellent fidelity and good electrical properties. A completed array is shown in Figure 11. Unfortunately, these devices did not exhibit electrical characteristics typical of transistors. Instead, the devices generally failed due to the formation of shorts to the gate or failed to conduct a detectable current under any bias. This behavior was most likely due to several shortcomings of the fabrication procedure, to which we now turn our attention.

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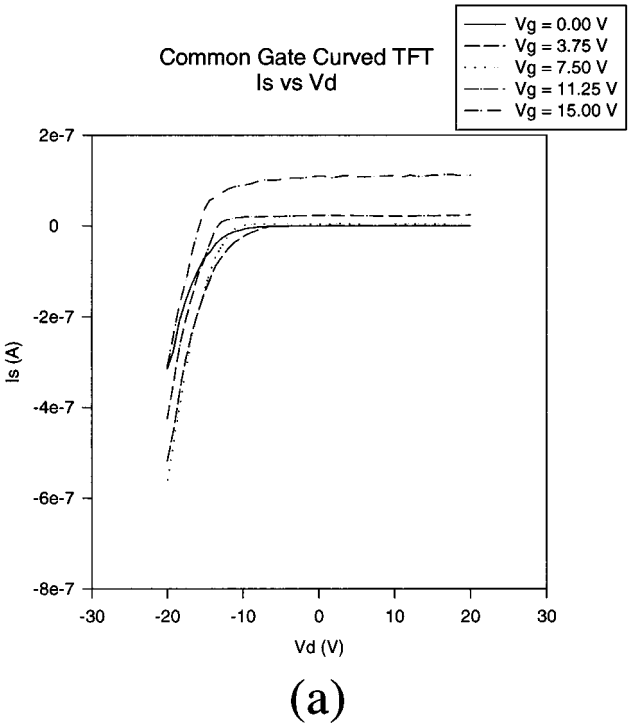

Figure 7. Electrical characteristics for common gate/channel TFT structures on a spherically curved glass substrate: (a) output curves; (b) transfer curves (gate current indicates leakage). In part b, a constant bias of 0.1 V was maintained on the drain contact with respect to the source to suppress source/drain current flow.

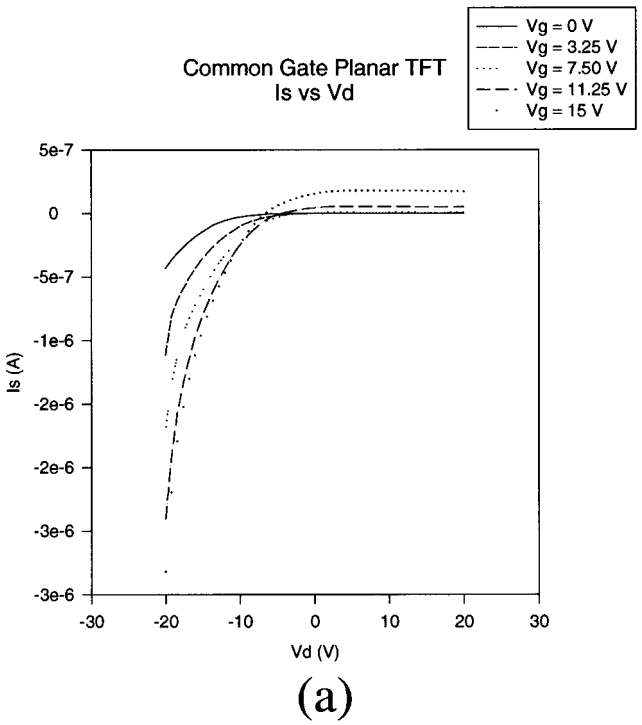

Figure 8. Electrical characteristics for common gate/channel TFT structures on a planar glass substrate: (a) output curves; (b) transfer curves (gate current indicates leakage). In part b, a constant bias of 0.1 V was maintained on the drain contact with respect to the source to suppress source/drain current flow.

First, the liftoff process used to remove the polymer template following each deposition step may have adversely affected the electrical behavior. As mentioned earlier, we used a commercially available polyurethane as our molded polymer template and lifted it off of the substrate using a CH_2Cl_2/CH_3OH solution. There have been reports of "dry" liftoff techniques, in which a polymer template is physically lifted from the surface rather than using a solvent solution to effect liftoff.[37] In our experience, dry liftoff can be done with these materials, but we did not find it to be a reliable general method for removing this polymer from the substrate, as it frequently resulted in incomplete template removal. Solvent-assisted liftoff works well in many instances, but we suspect that this liftoff process

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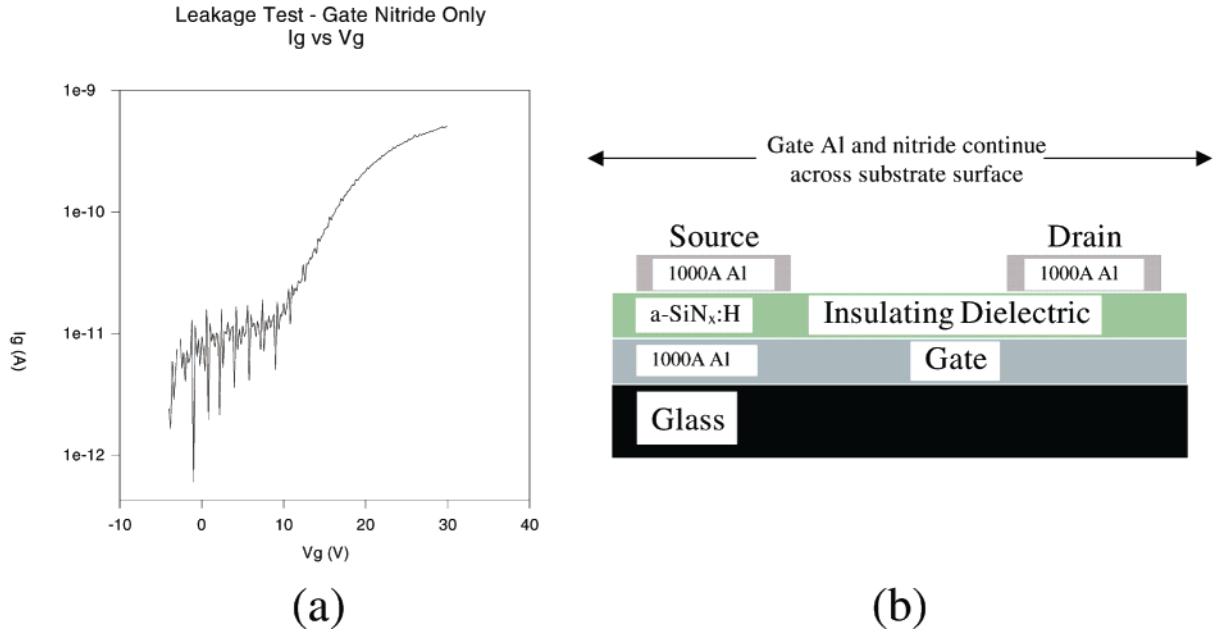

Figure 9. Direct measurement of leakage current through the gate nitride layer alone: (a) gate current vs gate voltage; (b) a cross-sectional schematic of the test structure used for the measurement. In part a, a constant bias of 0.1 V was maintained on the drain contact with respect to the source to suppress source/drain current flow.

adversely affected the electrical properties of the isolated channel TFT structures. For example, residual polymeric fringes are present along the edges of some device features even after liftoff, as can be seen in Figure 10b,d. Template liftoff can also remove material needed for devices to perform ideally. While such defects probably would not substantially degrade the electrical behavior of an entire array of common gate/channel TFTs in which the liftoff was performed only once on the topmost layer of the device, they could have a significant impact on isolated devices with multiple patterned layers in which liftoff-induced defects could be compounded with each successive patterning step. Previous TFT fabrication work based on photolithographic patterning suggests that using RIE to define the device features typically yields higher quality devices.[14,19] The reason that we did not use RIE or another etching method to isolate the devices is that MIMIC requires a continuous capillary path through the mold along which the liquid prepolymer can flow. Isolating devices by etching is incompatible with this requirement of MIMIC, since the etch template would require the formation of discrete polymeric resist structures. The differences in electrical behavior between devices isolated by liftoff and those isolated by etching certainly comprise a topic for further study, although because the issue is not specific to MIMIC, we did not pursue it further.

A second and probably more critical aspect of the fabrication that may have contributed to the degradation of the isolated channel devices' electrical properties is the thickness of the polymer template used to define the device features. The template thickness was measured by profilometry to be 30 μm, and in the SEM image shown in Figure 5b, it is clearly very thick compared to the thickness of the deposited trilayer films. As a result, the template shadowed the substrate from the deposition flux during film growth, an effect evident from the color gradient visible in Figure 10b,c.

The color gradient is indicative of a film thickness gradient near the edge of the TFT contact and channel regions. The channel region, being the narrowest and most critical part of the device, would be particularly susceptible and sensitive to film nonuniformity caused by shadowing, which could result in degradation due to an incomplete channel layer, undesirable contact between nonadjacent film layers, or varying electric field magnitudes within the device. This problem could be solved in principle by using a conformal deposition technique like low-temperature plasma-enhanced CVD, which can also yield high-quality a-Si and a-SiN_x films for use in TFTs.[38] Although decreasing the thickness of the polyurethane template would also serve to reduce the degree of shadowing during film deposition, the extent to which the thickness can be reduced depends on the following: (a) the aspect ratio required to maintain the integrity of the silicone mold (e.g., molds tend to sag if the aspect ratio is too low); (b) the throughput limitations imposed by changing the dimensions of the mold capillaries through which the liquid prepolymer flows, which will affect the flow rate; and (c) the resolution of the mask imaging technique.[3] We and others are currently working to develop methods which address these concerns, particularly by developing new inks which will allow ultrathin resist patterns to be laid down by microcontact printing (μCP).[30−31,39−52]

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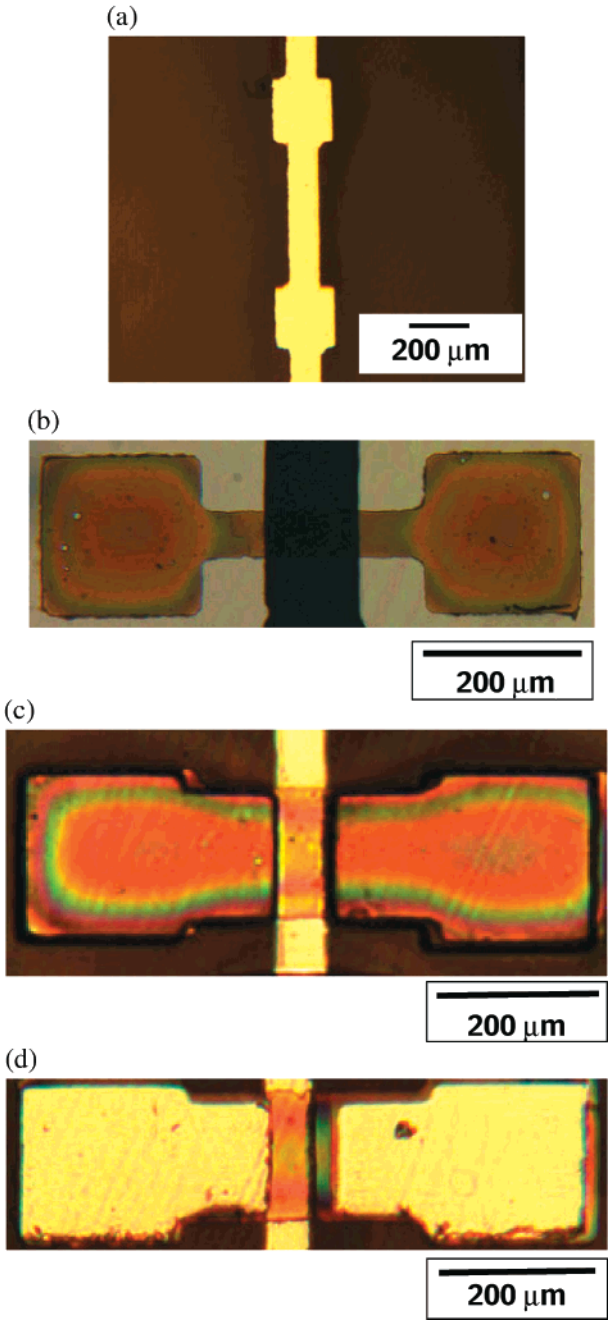

Figure 10. Optical micrographs showing isolated channel, inverted, staggered TFT microstructures following: (a) gate line metallization and liftoff of the polymer template (Figure 4d); (b) trilayer deposition and liftoff of the polymer template (Figure 4f); (c) etching of the passivation nitride (Figure 4h); (d) source/drain contact metallization (Figure 4j).

A final noteworthy aspect of this fabrication is that the polyurethane templates used in this study did not suffer in any noticeable way from the low-pressure, elevated-temperature, or reactive plasma environment inside the deposition chamber and were readily removed following trilayer deposition. Because many polymers decompose or degrade at higher temperatures, this relatively low-temperature reactive magnetron sputtering method is well-suited for use with polymer molding.

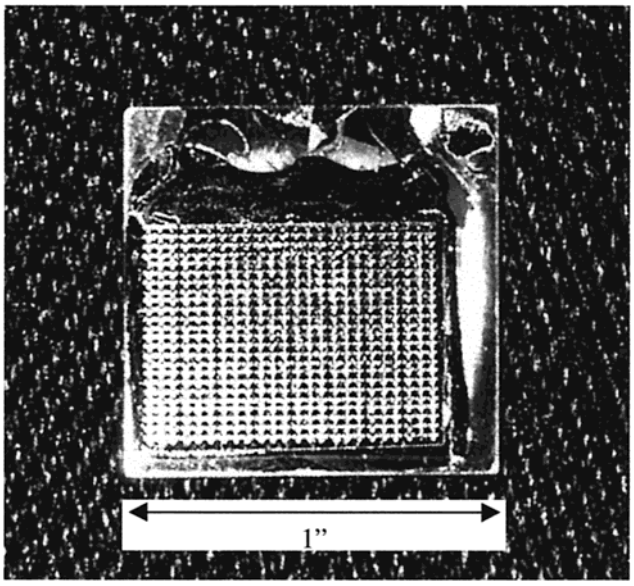

Figure 11. Completed array of isolated channel, inverted, staggered TFT microstructures on a planar glass substrate.

Taken together, the data suggest that MIMIC is an effective method for patterning complex thin-film devices on nonplanar substrates. There is no question that many engineering issues, from throughput to electrical performance optimization, have yet to be solved. This work, however, demonstrates that TFTs—a critical component of numerous sensor and display technologies—are compatible with novel patterning and film deposition techniques for use on substrates with three-dimensional curvature. The further development of these methods for this challenging application, especially in the areas of resist materials design and multilevel registration, appears to be an appropriate and timely subject for future research.

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